IN THE CLAIMS

1. (currently amended) A graphical profile map for integrated circuits on a substrate, the graphical profile map comprising an overlaid depiction of:
a top plane view of the entire substrate,
all die placement boundaries for the integrated circuits on the substrate,
all shot placement boundaries for the integrated circuits on the substrate, and
integrated circuit property information close-bounded contour lines, where the contour lines are not limited in placement to ~~either of~~ the die placement boundaries and the contour lines are not limited in placement to the shot placement boundaries.

2. (currently amended) The graphical profile map of claim 1, wherein the integrated circuit property information is provided from a database of historical integrated circuit property information when a desired amount of historical integrated circuit property information is available, and when the desired amount of historical integrated circuit property information is not available, ~~the~~ additional integrated circuit property information is provided by programmable algorithms.

3. (original) The graphical profile map of claim 2, wherein the programmable algorithms comprise modification algorithms and smoothing algorithms and the algorithms are implemented by at least one of manually by an engineer, automatedly by an intelligent agent, and automatedly by an intelligent script.

4. (original) The graphical profile map of claim 1, wherein the graphical profile map is stored as an image file on a computer readable media.

5. (original) The graphical profile map of claim 1, wherein the integrated circuit property information comprises composite integrated circuit property information for all processes that the integrated circuits have undergone.

6. (original) The graphical profile map of claim 1, wherein the integrated circuit property information comprises integrated circuit property information for a selectable single process that the integrated circuits have undergone.

7. (original) The graphical profile map of claim 1, wherein the integrated circuit property information comprises integrated circuit property information for a selectable subset of processes that the integrated circuits have undergone.

8. (original) The graphical profile map of claim 1, wherein the integrated circuit property information is presented by representing different integrated circuit property information value ranges with different colors.

9. (original) The graphical profile map of claim 1, wherein the integrated circuit property information comprises yield information.

10. (original) The graphical profile map of claim 1, wherein the shot placement boundaries comprise a graphical shot grid representation.

11. (original) The graphical profile map of claim 1, wherein the die placement boundaries comprise a graphical die grid representation.

12. (original) The graphical profile map of claim 1, further comprising a graphical indication depicting an offset from a center of the substrate to a center of a closest unit of the shot placement boundaries.

13. (canceled)
14. (canceled)
15. (canceled)
16. (canceled)
17. (canceled)
18. (canceled)
19. (canceled)
20. (canceled)